What is claimed is:

1. A method comprising:

producing in a first engine thread included in a processor that processes packets, a vector that represents content of a packet; and

storing the vector in a memory associated with the processor such that the vector is accessible by a second engine thread included in the processor.

2. The method of claim 1, wherein producing the vector includes grouping and summing the content of the packet to produce vector elements.

3. The method of claim 1, further comprising:

updating the vector on the second engine thread included in the processor.

4. The method of claim 3, further comprising:

storing the updated vector in the memory such that the updated vector is accessible by a third engine thread included in the processor.

5. The method of claim 1, wherein the vector is representable as $C = (C_1, C_2, \ldots, C_n) = \left(\sum_i B_{i,1}, \sum_i B_{i,2}, \ldots, \sum_i B_{i,n} \right)$.

6. The method of claim 3, wherein updating the vector includes subtracting a byte from an element included in the vector.

7. The method of claim 3, wherein updating the vector includes rotating elements included in the vector.

8. The method of claim 3, wherein the updated vector is used to determine a numerical value that represents the content of the packet.

9. The method of claim 8, wherein the numerical value is inserted into the packet.

10. The method of claim 8, wherein the numerical value is used to verify payload of the packet.

11. A computer program product, tangibly embodied in an information carrier, for monitoring content of a packet, the computer program product being operable to cause a machine to:

produce in a first engine thread included in a processor that processes packets, a vector that represents content of the packet; and

store the vector in a memory associated with the processor such that the vector is accessible by a second engine thread included in the processor.

12. The computer program product of claim 11, wherein producing the vector includes grouping and summing the content of the packet to produce vector elements.

13. The computer program product of claim 11 being further operable to cause a machine to:

update the vector on the second engine thread included in the processor.

14. The computer program product of claim 13 being further operable to cause a machine to:

store the updated vector in the memory such that the updated vector is accessible by a third engine thread included in the processor.

15. The computer program product of claim 11, wherein the vector is representable as $C=(C_1,C_2,\ldots,C_n)=\left(\sum_i B_{i,1},\sum_i B_{i,2},\ldots,\sum_i B_{i,n}\right)$.

16. The computer program product of claim 13, wherein updating the vector includes subtracting a byte from an element included in the vector.

17. The computer program product of claim 13, wherein updating the vector includes rotating elements included in the vector.

18. The computer program product of claim 13, wherein the updated vector is used to determine a numerical value that represents the content of the packet.

19. The computer program product of claim 18, wherein the numerical value is inserted into the packet.

20. The computer program product of claim 18, wherein the numerical value is used to verify payload of the packet.

21. A packet verifier comprises:

a process to produce in a first engine thread included in a processor that processes packets, a vector that represents content of a packet; and

a process to store the vector in a memory associated with the processor such that the vector is accessible by a second engine thread included in the processor.

22. The packet verifier of claim 21, wherein producing the vector includes grouping and summing the content of the packet to produce vector elements.

23. The packet verifier of claim 21, further comprises:

a process to update the vector on the second engine thread included in the processor.

24. The packet verifier of claim 23, further comprises:

a process to store the updated vector in the memory such that the updated vector is accessible by a third engine thread included in the processor.

25. The packet verifier of claim 21, wherein the vector is representable as $C=(C_1,C_2,\ldots,C_n)=\left(\sum_i B_{i,1},\sum_i B_{i,2},\ldots,\sum_i B_{i,n}\right)$.

26. The packet verifier of claim 23, wherein updating the vector includes subtracting a byte from an element included in the vector.

27. The packet verifier of claim 23, wherein updating the vector includes rotating elements included in the vector.

28. The packet verifier of claim 23, wherein the updated vector is used to determine a numerical value that represents the content of the packet.

29. The packet verifier of claim 28, wherein the numerical value is inserted into the packet.

30. The packet verifier of claim 28, wherein the numerical value is used to verify payload of the packet.

31. A system comprising:

a network processor capable of,

producing in a first engine thread included in the network processor, a vector that represents content of a packet, and

storing the vector in a memory associated with the processor such that the vector is accessible by a second engine thread included in the network processor.

32. The system of claim 31, wherein producing the vector includes grouping and summing the content of the packet to produce vector elements.

33. The system of claim 31, wherein the network processor is further capable of:

updating the vector on the second engine thread included in the network processor.

34. A network forwarding device comprising:

an input port for receiving packets;

an output for delivering the received packets; and

a network processor capable of,

producing in a first engine thread included in the network processor, a vector that represents content of a packet, and

storing the vector in a memory associated with the network processor such that the vector is

accessible by a second engine thread included in the network processor.

35. The system of claim 34, wherein producing the vector includes grouping and summing the content of the packet to produce vector elements.

36. The system of claim 34, wherein the network processor is further capable of updating the vector on the second engine thread included in the network processor.

37. A method comprising:

grouping and summing content of a packet to produce elements of a vector that represents the content of the packet; and

storing the vector in a memory associated with a processor such that the vector is accessible.

38. The method of claim 37, further comprising:

updating the vector to reflect processing of the content of the packet.

39. The method of claim 37, wherein the vector is representable as $C=(C_1,C_2,\ldots,C_n)=\left(\sum_i B_{i,1},\sum_i B_{i,2},\ldots,\sum_i B_{i,n}\right)$.